

L Number	Hits	Search Text	DB	Time stamp
1	70293	flash with memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 09:51
2	100841	dram (dynamic with ram)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 09:51
3	15756	(flash with memory) and (dram (dynamic with ram))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 09:52
4	2532735	chip die semiconductor ic (integrated adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 09:52
5	4224	(flash with memory) same (dram (dynamic with ram)) same (chip die semiconductor ic (integrated adj circuit))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 09:53
6	383	((stacked stack stacking stackable multi multilevel) same ((flash with memory) same (dram (dynamic with ram)) same (chip die semiconductor ic (integrated adj circuit))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 09:54
7	206	((package packaging packaged) and ((stacked stack stacking stackable multi multilevel) same ((flash with memory) same (dram (dynamic with ram)) same (chip die semiconductor ic (integrated adj circuit))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 09:54
8	41	((interposed spacer interpose) and ((package packaging packaged) and ((stacked stack stacking stackable multi multilevel) same ((flash with memory) same (dram (dynamic with ram)) same (chip die semiconductor ic (integrated adj circuit))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 09:58
9	165	((package packaging packaged) and ((stacked stack stacking stackable multi multilevel) same ((flash with memory) same (dram (dynamic with ram)) same (chip die semiconductor ic (integrated adj circuit)))) not ((interposed spacer interpose) and ((package packaging packaged) and ((stacked stack stacking stackable multi multilevel) same ((flash with memory) same (dram (dynamic with ram)) same (chip die semiconductor ic (integrated adj circuit))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 09:58

L Number	Hits	Search Text	DB	Time stamp
1	2	6642627.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 06:56
2	2532735	chip die semiconductor ic (integrated adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 06:57
3	6	(semiconductor si silicon gaas) with subsstrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 06:58
4	560743	(semiconductor si silicon gaas) with substrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 06:58
5	560744	((semiconductor si silicon gaas) with subsstrate) ((semiconductor si silicon gaas) with substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 06:59
6	103320	cell with region	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 07:00
7	11439	(chip die semiconductor ic (integrated adj circuit)) same (((semiconductor si silicon gaas) with subsstrate) ((semiconductor si silicon gaas) with substrate)) same (cell with region)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 07:01
8	64311	(wiring bond rearrangement pattern) with pad	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 07:03
9	98	((chip die semiconductor ic (integrated adj circuit)) same (((semiconductor si silicon gaas) with subsstrate) ((semiconductor si silicon gaas) with substrate)) same (cell with region)) same ((wiring bond rearrangement pattern) with pad)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 07:32
10	1		USPAT	2004/06/25 07:10
11	1		USPAT	2004/06/25 07:10
12	1		USPAT	2004/06/25 07:10
13	1		USPAT	2004/06/25 07:10
14	1		USPAT	2004/06/25 07:12
15	1		USPAT	2004/06/25 07:13
16	1		USPAT	2004/06/25 07:13
17	1		USPAT	2004/06/25 07:14
18	1		USPAT	2004/06/25 07:14
19	1		USPAT	2004/06/25 07:14
20	1		USPAT	2004/06/25 07:14

21	1		USPAT	2004/06/25 07:14
22	1		USPAT	2004/06/25 07:15
23	1		USPAT	2004/06/25 07:15
24	1		USPAT	2004/06/25 07:16
25	1		USPAT	2004/06/25 07:16
26	1		USPAT	2004/06/25 07:17
27	1		USPAT	2004/06/25 07:18
28	1		USPAT	2004/06/25 07:18
29	1		USPAT	2004/06/25 07:19
30	1		USPAT	2004/06/25 07:19
31	578	((chip die semiconductor ic (integrated adj circuit)) same (((semiconductor si silicon gaas) with subsstrate) ((semiconductor si silicon gaas) with substrate)) same (cell with region)) and ((wiring bond rearrangement pattern) with pad)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 07:32
32	480	((chip die semiconductor ic (integrated adj circuit)) same (((semiconductor si silicon gaas) with subsstrate) ((semiconductor si silicon gaas) with substrate)) same (cell with region)) and ((wiring bond rearrangement pattern) with pad)) not (((chip die semiconductor ic (integrated adj circuit)) same (((semiconductor si silicon gaas) with subsstrate) ((semiconductor si silicon gaas) with substrate)) same (cell with region)) same ((wiring bond rearrangement pattern) with pad))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/25 07:32

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